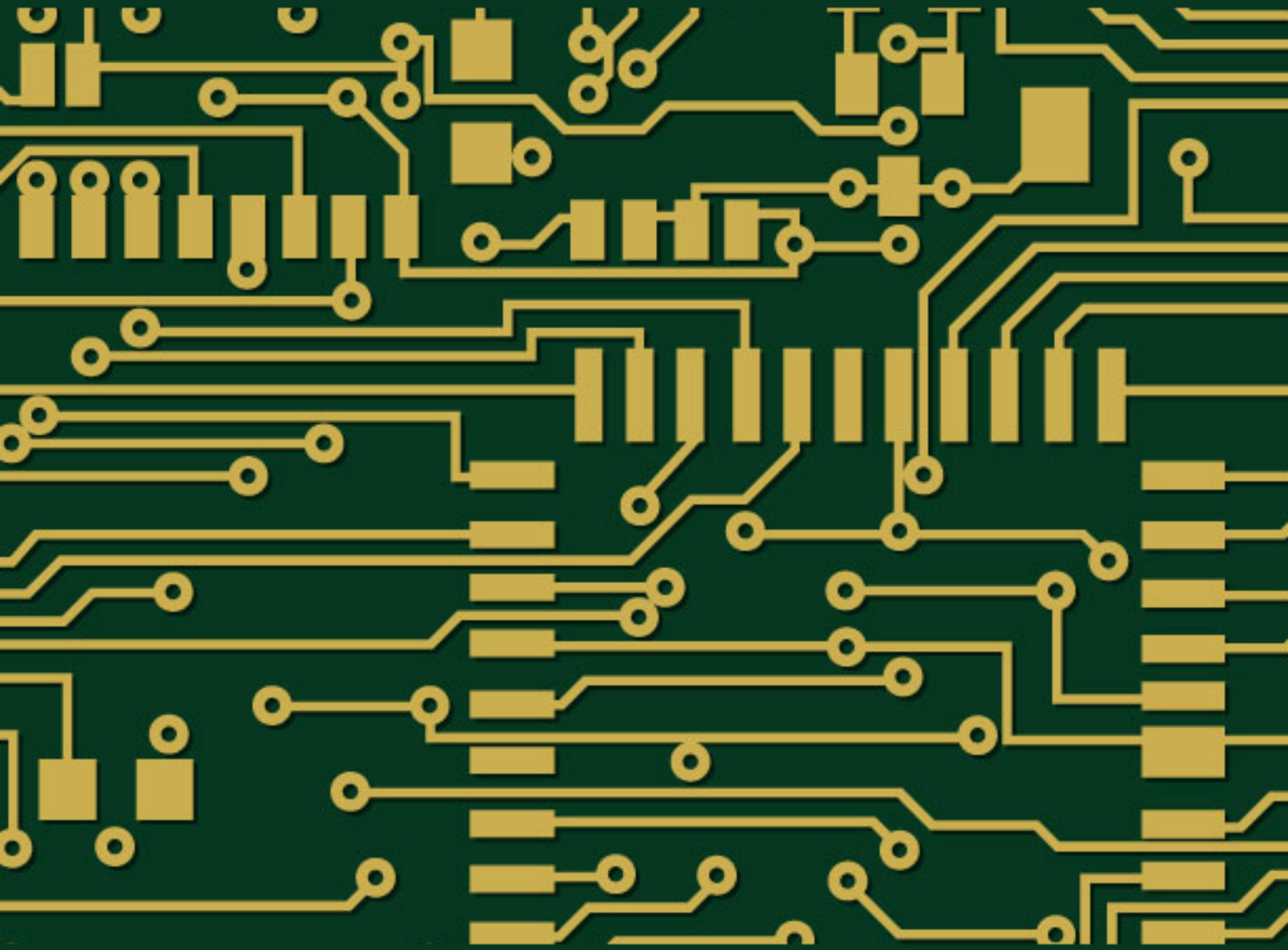
VTU eNotes On

Micro Electronics Circuits



(Electronics and Communication)

MODIFIED SYLLABUS

B.E. Electronics & Communication Engineering (2010-11Scheme)

Modified Syllabus (VI Semester)

MICROELECTRONICS CIRCUITS

Subject Code	: **10EC63**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

PART A

UNIT – 1

MOSFETS: Device Structure and Physical Operation, V-I Characteristics, MOSFET Circuits at DC, Biasing in MOS amplifier Circuits, Small Signal Operation and Models, MOSFET as an amplifier and as a switch, biasing in MOS amplifier circuits, small signal operation modes, single stage MOS amplifiers. SPICE MOSFET Examples. **8 Hrs**

UNIT -2

Single Stage IC Amplifier: IC Design philiosophy, CoUmparison of MOSFET and BJT, Current sources, Current mirrors and Current steering circuits, high frequency response. 5 **Hrs**

UNIT – 3

Single Stage IC amplifiers (continued): CS and CF amplifiers with loads, high frequency response of CS and CF amplifiers, CG and CB amplifiers with active loads, high frequency response of CG and CB amplifiers, Cascade amplifiers. CS and CE amplifiers with source (emitter) degeneration source and emitter followers, some useful transfer parings, current mirrors with improved performance. SPICE examples. **7 Hrs**

UNIT – 4

Differences and Multistage Amplifiers: The MOS differential pair, small signal operation of MOS differential pair, the BJT differences pair, other non-ideal characteristics and differential pair, Differential amplifier with active loads, frequency response and differential amplifiers. Multistage amplifier. SPICE examples. **8 Hrs**

PART B

UNIT – 5

Feedback. General Feedback structure. Properties of negative feedback. Four basic feedback topologies. Series-Shunt feedback. Determining the loop gain. Stability problem. Effect of feedback an amplifier poles. Stability study using Bode plots. Frequency compensation. SPICE examples. **8 Hrs**

UNIT - 6

Operational Amplifiers: Ideal Op-amp, Inverting Configuration, Non-inverting Configuration, Difference Amplifiers, Open-Loop Gain & BW on Circuit Perforamnce, Large signal peration of Op-Amps, DC Imperfections, Integratior & Differentiatiors, Non-linear Function Oprations, Sample and Hold Circuit, The SPICE Eamples. **9 Hrs**

UNIT – 7

Digital CMOS circuits. Overview. Design and performance analysis of CMOS inverter. Logic Gate Circuits. Pass-transistor logic. Dynamic Logic Circuits. SPICE examples. **7 Hrs**

Text Book:

1. **"Microelectronic Circuits",** Adel Sedra and K.C. Smith, 5th Edition, Oxford University Press, Interantional Version, 2009.

Reference Book:

1. **"Fundamentals of Microelectronics"** , Behzad Razavi, John Wiley India Pvt. Ltd, 2008.
2. **"Microelectronics – Analysis and Design"**, Sundaram Natarajan, Tata McGraw-Hill, 2007

Note : Unit1, Unit 2, Unit3 & Unit 4 - Can be of 5 questions.
Unit 5, Unit 6, & Unit 7 - Can be of 3 questions.

Unit 1 ï Chapter 4
MOS Field-Effect Transistors (MOSFETs)

UNIT 1 OUTLINE

1.1 Device Structure and Physical Operation
1.2 Current ï Voltage Characteristics
1.3 MOSFET Circuits at DC
1.4 Biasing in MOS amplifier circuits
1.5 Small Signal Operation and Models
1.6 The MOSFET as an Amplifier and as a Switch
1.7 Single Stage MOS amplifiers
1.8 SPICE MOSFET models and examples

LEARNING OUTCOMES:
At the end of this chapter one can clearly get to know the following:

- **Understanding Physical construction and operation of an Enhancement MOSFET**
- **Drawing the V-I characteristics of n and p channel E-MOSFET**
- **DC operation or biasing of MOSFETs**
- **AC Operation: Small signal modeling of MOSFETs**
- **Single stage MOS amplifiers : Common Source, Common Drain and Common Gate amplifiers**
- **SPICE modeling of MOSFETs**

INTRODUCTION

Along with the Junction Field Effect Transistor (JFET), there is another type of Field Effect Transistor available whose Gate input is electrically insulated from the main current carrying channel and is therefore called an **Insulated Gate Field Effect Transistor** or **IGFET**. The most common type of insulated gate FET which is used in many different types of electronic circuits is called the **Metal Oxide Semiconductor Field Effect Transistor** or **MOSFET** for short.

The **IGFET** or **MOSFET** is a voltage controlled field effect transistor that differs from a JFET in that it has a "Metal Oxide" Gate electrode which is electrically insulated from the main semiconductor N-channel or P-channel by a thin layer of insulating material usually silicon dioxide (commonly known as glass). This insulated metal gate electrode can be thought of as one plate of a capacitor. The isolation of the controlling Gate makes the input resistance of the **MOSFET** extremely high in the Mega-ohms (MΩ) region thereby making it almost infinite.

As the Gate terminal is isolated from the main current carrying channel "NO current flows into the gate" and just like the JFET, the **MOSFET** also acts like a voltage controlled resistor were the current flowing through the main channel between the Drain and Source is proportional to the input voltage. Also like the JFET, this very high input resistance can easily accumulate large amounts of static charge resulting in the **MOSFET** becoming easily damaged unless carefully handled or protected.

MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available. The main difference this time is that MOSFETs are available in two basic forms:

1. **Depletion Type** - the transistor requires the Gate-Source voltage, (V_{GS}) to switch the device "OFF". The depletion mode MOSFET is equivalent to a "Normally Closed" switch.

2. **Enhancement Type** - the transistor requires a Gate-Source voltage, (V_{GS}) to switch the device "ON". The enhancement mode MOSFET is equivalent to a "Normally Open" switch.

Basic operating principle of a MOSFET:

- **Use of the voltage between two terminals to control the current flowing in the third terminal**
- **Also, the control signal can be used to cause the current in the third terminal to change from zero to a large value, thus allowing the device to act as a switch.**

The FET differs from BJT in the following important characteristics:

1. It is a unipolar device
2. It is simpler to fabricate
3. Occupies less space in Integrated form, packaging density is high(>200 million)
4. It has higher input resistance
5. It can be used as a symmetrical Bilateral switch
6. It functions as a memory device
7. It is less noisy than a BJT
8. It exhibits no offset voltage at zero input, hence making an excellent signal chopper

THE ONLY DISADVANTAGE IS IT HAS SMALLER GAIN- BANDWIDTH PRODUCT THAN BJT

The symbols and basic construction for both configurations of MOSFETs are shown below.

DEVICE STRUCTURE AND PHYSICAL OPERATION

Device Structure:

Figure 4.1 shows the physical structure of the n-channel enhancement-type MOSFET. The transistor is fabricated on a p-type substrate. Two heavily doped n-type regions: the *n*+ source and the *n*+ drain regions, are created in the substrate.

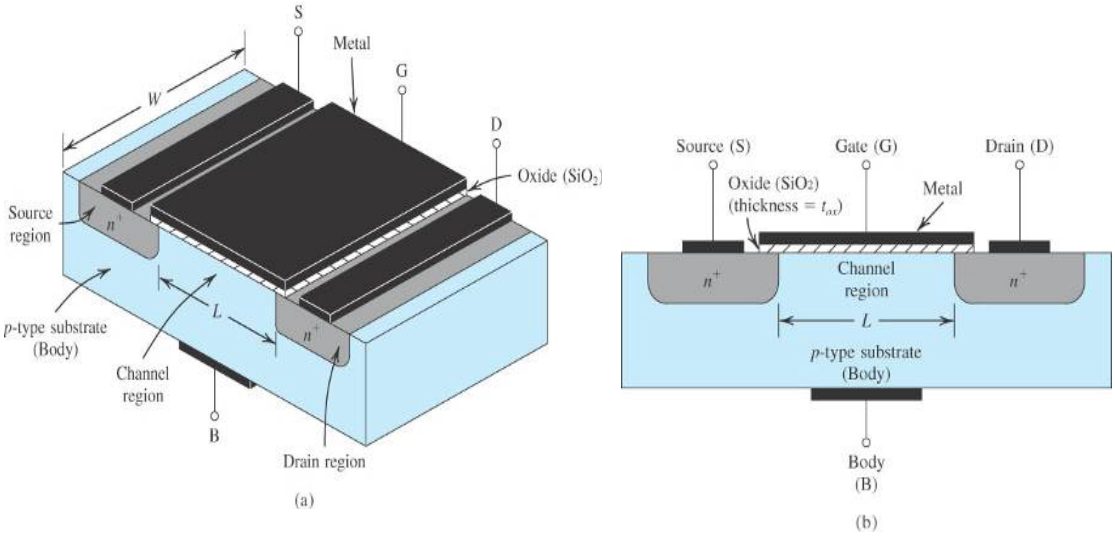


Figure 1. Physical structure of the enhancement-type NMOS transistor: (a)Perspective view; (b)Cross-section. Typically *L*= 0.1 to 3 Õm, *W*= 0.2 to 100 Õm, and the thickness of the oxide layer (t*ox*) is in the range of 2 to 50 nm.

1. A thin layer of silicon dioxide (SiO2) of thickness *tox* (typically 2-50 nm) - an excellent electrical insulator, is grown on the surface of the substrate, in the area between the source and drain regions.
2. Metal is deposited on top of the oxide layer to form the **gate electrode.**
3. Metal contacts are also made to the source region, the drain region, and the substrate, also known as the **body**.

Thus four terminals are brought out: the gate terminal (G), the source terminal (S), the drain terminal (D), and the substrate or body terminal (B).

A voltage applied to the gate of the MOSFET controls current flow between source and drain. This current will flow in the longitudinal direction from drain to source in the region labelled **ñchannel region.ò**
This region has a length L in the range of 0.1 μm to 3 μm, and a width W in the range of 0.2 μm to 100 μm.

Note: The MOSFET is a symmetrical device [its source and drain can be interchanged with no change in device characteristics].

Device Operation:

(i) With No Gate Voltage

With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source. They prevent current conduction from drain to source when a voltage V_{DS} is applied. The path between drain and source has a very high resistance (of the order of $10^{12}\Omega$).

(ii) Creating a Channel for Current Flow

The source and the drain are grounded and a positive voltage is applied to the gate.
The positive voltage on the gate causes the free holes (which are positive charged) to be repelled from the region of the substrate under the gate. These holes are pushed downward into the substrate, leaving behind a carrier-depletion region as shown below.

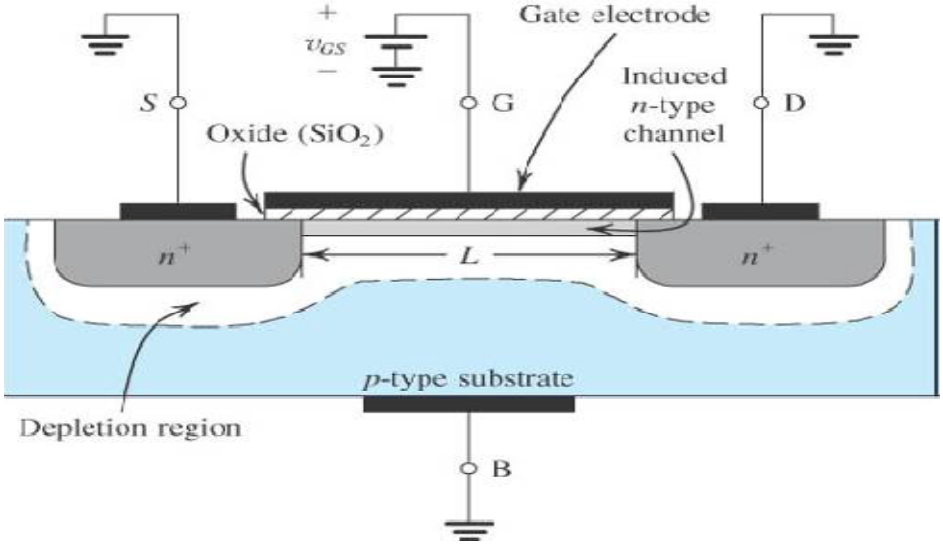


Figure 4.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

The positive gate voltage attracts electrons from the *n*+ source and drain regions into the channel region. When a sufficient number of electrons accumulate near the surface of the substrate under the gate, an n region is in effect created, connecting the source and drain regions, as indicated in Fig. 4.2. This MOSFET is called an **n-channel MOSFET** or, alternatively, an **NMOS transistor**. The induced channel is also called an **inversion layer**. The induced *n* region thus forms a **channel** for current flow from drain to source.

Note: **The value of V_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the threshold voltage and is denoted V_t.**

The value of V_t is controlled during device fabrication and typically lies in the range of 0.5 V to 1.0V.

Now if a voltage is applied between drain and source, current flows through this induced n region.

The gate and the channel region of the MOSFET form a parallel-plate capacitor, with the oxide layer acting as the capacitor dielectric. An electric field thus develops in the vertical direction. It is this field that controls the amount of charge in the channel, and thus it determines the channel conductivity and, in turn, the current that will flow through the channel when a voltage v_{DS} is applied.

$$V_{OV} \equiv v_{GS} - V_t \text{ (effect voltage, or overdrive voltage)}$$

$$V_t : \text{Threshold voltage,}$$

$$\text{Typically lies in the range of 0.3V to 1.0V}$$

The magnitude of the electron charge in the channel by

$$|Q| = C_{ox} V_{OV} \underbrace{WL}_{A}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \begin{cases} C_{ox} : \text{The capacitance per unit gate area,} \\ \quad \text{called the oxide capacitance} \\ \varepsilon_{ox} : \text{the permittivity of the silicon oxide,} \\ \quad \varepsilon_{ox} = 3.9\varepsilon_0 = 3.45 \cdot 10^{-11} \text{F/m} \\ t_{ox} : \text{the thickness of the oxide} \end{cases}$$

(iii) Effect of Applying a Small V_{DS}

We now apply a small positive voltage V_{DS} between drain and source, as shown in Fig. 4.3.

- The voltage v_{DS} causes a current i_D to flow through the induced n channel. Current is carried by free electrons traveling from source to drain.
- The magnitude of i_D depends on the density of electrons in the channel, which in turn depends on the magnitude of v_{DS}
- Specifically, for $v_{GS} = V_t$, more electrons are attracted into the channel.
- The result is a channel of increased conductance or, equivalently, reduced resistance. In fact, the conductance of the channel is proportional to the excess gate voltage(v_{GS}-V_t), also known as the effective voltage or the overdrive voltage.
- Figure 4.4 shows a sketch of i_D versus v_{DS} for various values of v_{GS}. We observe that the MOSFET is operating as a linear resistance whose value is controlled by v_{GS}.

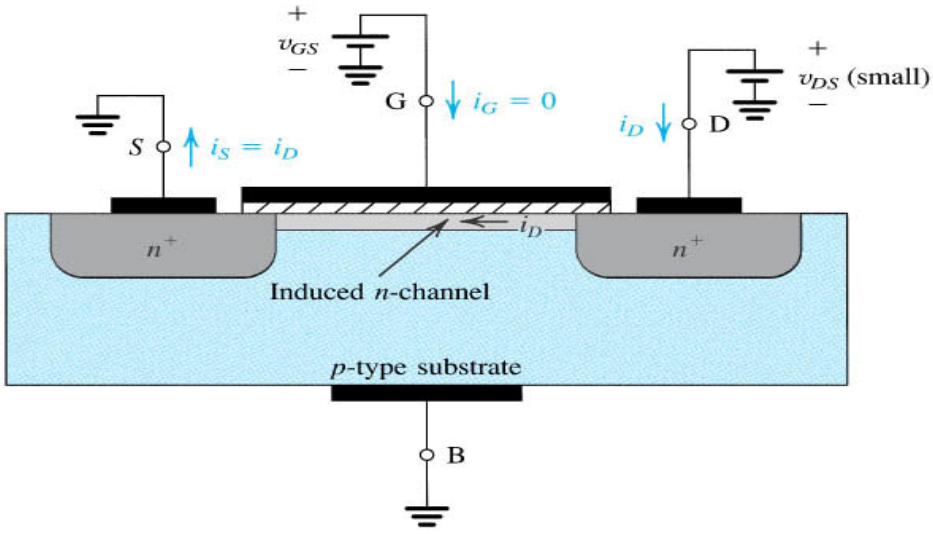


Figure 4.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS} (depletion region not shown).

- The resistance is infinite for $v_{GS} \leq V_t$, and its value decreases as v_{GS} exceeds V_t.
- Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)\, v_{DS}$.
- Then, increasing v_{GS} above the threshold voltage V_t enhances the channel, hence the name **enhancement-mode operation** and **enhancement-type MOSFET.** Finally, we note that the current that leaves the source terminal (i_S) is equal to the current that enters the drain terminal (i_D), and the gate current $i_G = 0$.

The expression for the channel resistance can be determined as follows:

- The charge per unit channel lenth as

$$\frac{|Q|}{\text{unit channel lenth}} = \frac{C_{ox} V_{OV} W L}{L} = C_{ox} V_{OV} W$$

- The electron field E across the lenth of channel as

$$|E| = \frac{v_{DS}}{L}$$

- The electron drift velocity $= \mu_n |E| = \mu_n \dfrac{v_{DS}}{L}$

- The value of i_D can now be found by multiplying the charge per unit channel lenth by The electron drift velocity

$$i_D = C_{ox} V_{OV} W \times \mu_n \frac{v_{DS}}{L} = \left[\mu_n C_{ox} \frac{W}{L} V_{OV} \right] v_{DS}$$

$$i_D = \left[\mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t) \right] v_{DS}$$

- The Conductance $\frac{i_D}{v_{DS}} = g_{DS} = \mu_n C_{ox} \frac{W}{L}(v_{GS} - V_t)$
- k_n' : Process transconductance parameter, $k_n' = \mu_n C_{ox}$
- k_n : MOSFET transconductance parameter,

$$k_n = k_n'(W/L) = \mu_n C_{ox}(W/L)$$

- An NMOSFET with $v_{GS} > V_t$, and with a small v_{DS} applied, the MOSFET behaves as a linear resistance r_{DS} whose value is controlled by the gate voltage v_{GS}

$$r_{DS} = \frac{1}{g_{DS}} = \frac{1}{\mu_n C_{ox}(W/L)(v_{GS} - V_t)}$$

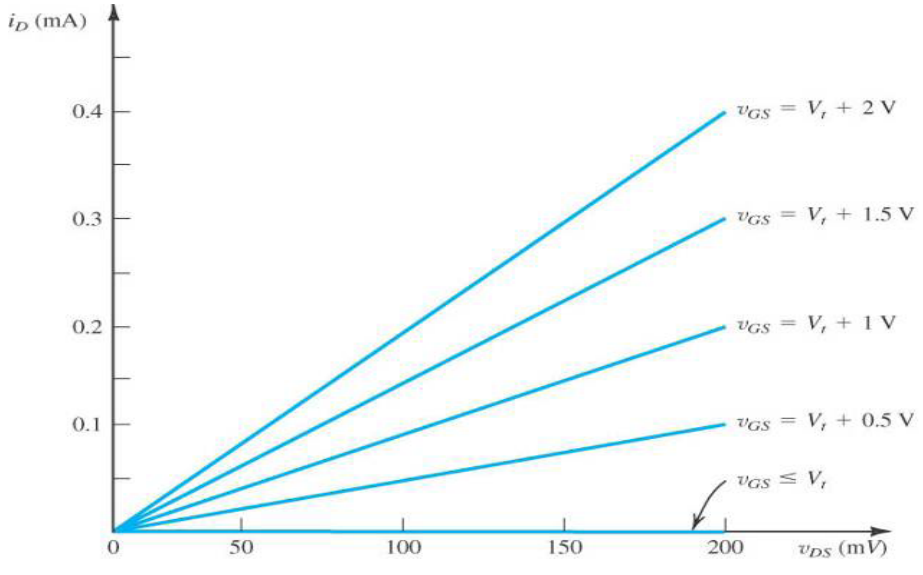


Figure 4.4 The i_D–v_{DS} characteristics of the MOSFET in Fig. 4.3 when the voltage applied between drain and source, v_{DS}, is kept small. The device operates as a linear resistor whose value is controlled by v_{GS}.

(iv) Operation as v_{DS} Is Increased

Å As we travel along the channel from source to drain, the voltage (measured relative to the source) increases from 0 to v_{DS}.

Å Thus the voltage between the gate and points along the channel decreases from v_{GS} at the source end to v_{GS}ï v_{DS} at the drain end.

Å Since the channel depth depends on this voltage, we find that the channel is no longer of uniform depth. As v_{DS} is increased, the channel becomes more tapered and its resistance increases correspondingly.

- When v_{DS} is increased to the value that reduces the voltage between gate and channel at the drain end to Vt ,

  $v_{GD} = V_t$ or $v_{GS} - v_{DS} = V_t$ or $v_{DS} = v_{GS} - V_t$

  the channel depth at the drain end decreases to almost zero, and the channel is said to be **pinched off.**
- As the value reached for $v_{DS} = v_{GS} - V_t$, the drain current **saturates**, and the MOSFET is said to have entered the saturation region of operation.

  $$v_{DSsat} = v_{GS} - V_t \qquad (4.1)$$
- The region of the $i_D - v_{DS}$ characteristic obtained for $v_{DS} < v_{DSsat}$ is called the **triode region.**

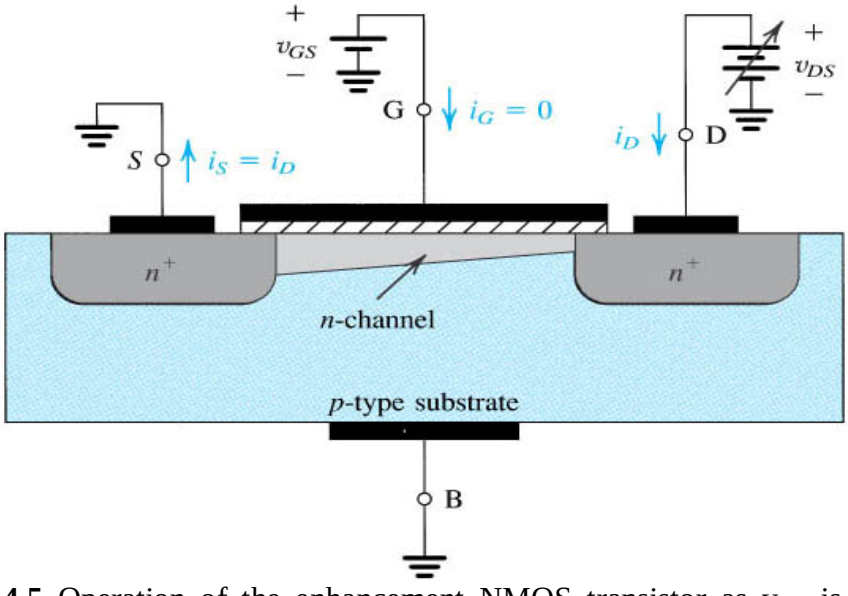


Figure 4.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t.

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