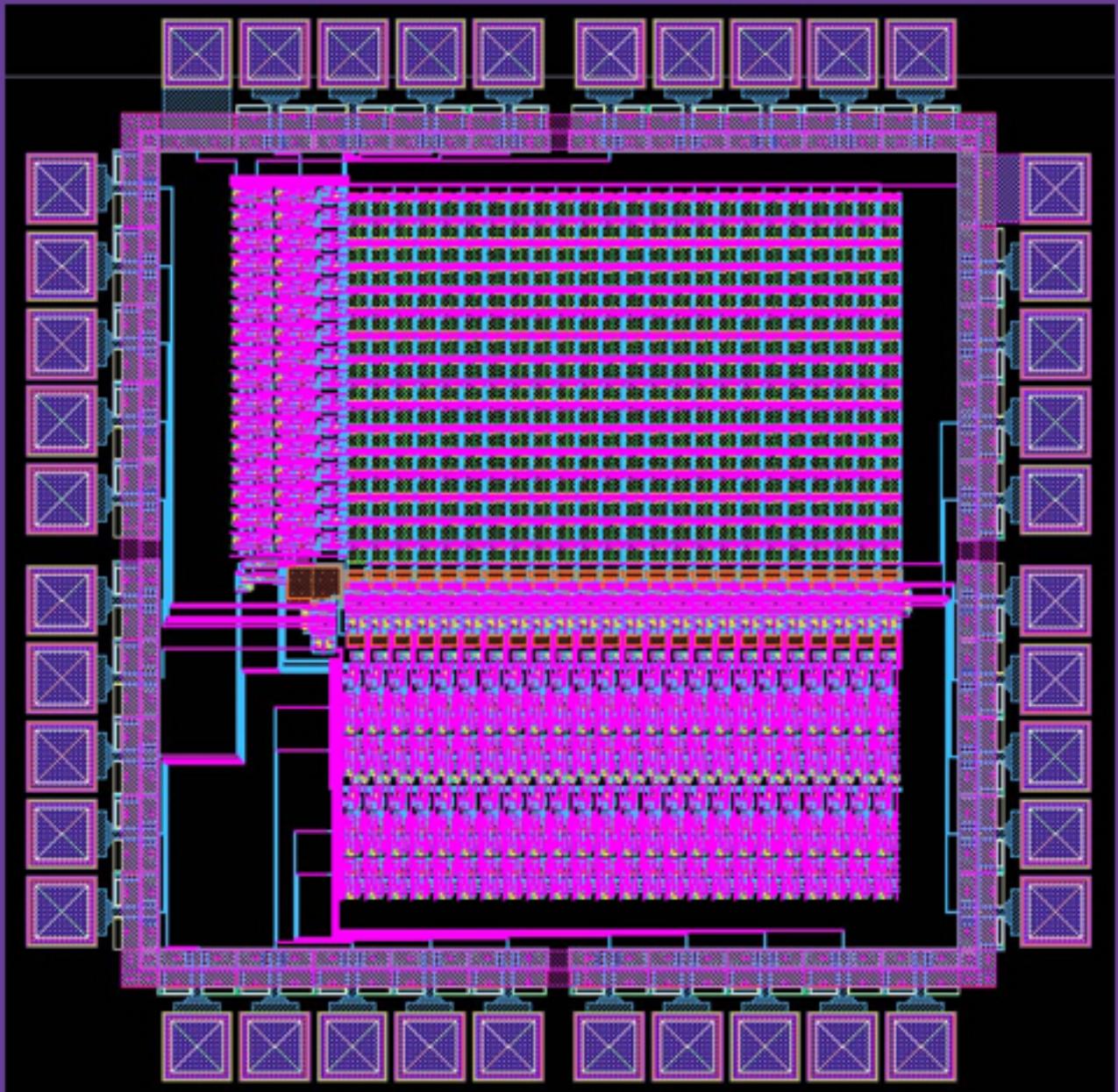


# VTU eNotes On

## Fundamentals of CMOS VLSI



**(Electronics and Communication)**

# MOS TRANSISTOR THEORY

## Introduction

A MOS transistor is a majority-carrier device, in which the current in a conducting channel between the source and the drain is modulated by a voltage applied to the gate.

Symbols

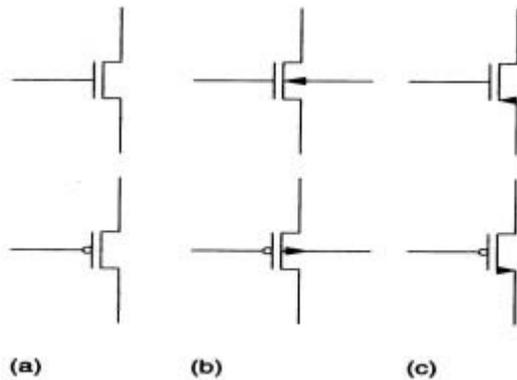


Figure 1 : symbols of various types of transistors.

## NMOS (n-type MOS transistor)

- (1) Majority carrier = electrons
- (2) A positive voltage applied on the gate with respect to the substrate enhances the number of electrons in the channel and hence increases the conductivity of the channel.
- (3) If gate voltage is less than a threshold voltage  $V_t$ , the channel is cut-off (very low current between source & drain).

## PMOS (p-type MOS transistor)

- (1) Majority carrier = holes
- (2) Applied voltage is negative with respect to substrate.

## Relationship between $V_{gs}$ and $I_{ds}$ , for a fixed $V_{ds}$ :

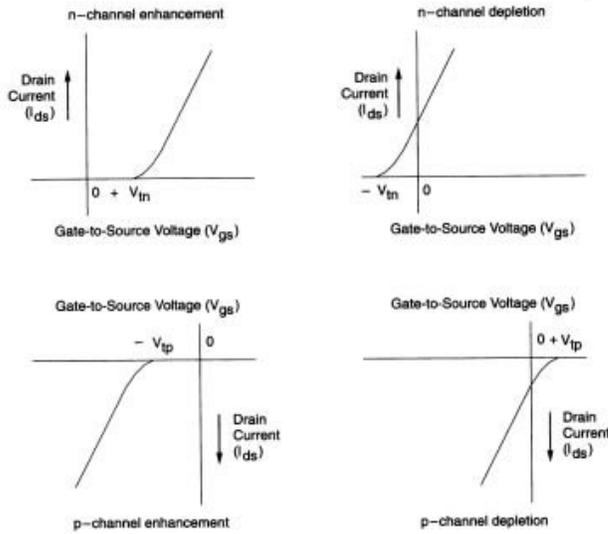


Figure 2: graph of  $V_{gs}$  vs  $I_{ds}$

Devices that are normally cut-off with zero gate bias are classified as "**enhancement-mode**" devices.

Devices that conduct with zero gate bias are called "**depletion-mode**" devices.

Enhancement-mode devices are more popular in practical use.

### Threshold voltage ( $V_t$ ):

The voltage at which an MOS device begins to conduct ("turn on"). The **threshold voltage** is a function of

- (1) Gate conductor material
- (2) Gate insulator material
- (3) Gate insulator thickness
- (4) Impurity at the silicon-insulator interface
- (5) Voltage between the source and the substrate  $V_{sb}$
- (6) Temperature

### MOS equations (Basic DC equations):

Three MOS operating regions are: Cutoff or subthreshold region, linear region and saturation region.

The following equation describes all these three regions:

$$I_{ds} = \begin{cases} 0; & V_{gs} - V_t \leq 0 \text{ cut-off} \\ \beta \left[ (V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2} \right]; & 0 < V_{ds} < V_{gs} - V_t \text{ linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2; & 0 < V_{gs} - V_t < V_{ds} \text{ saturation} \end{cases}$$

where  $\beta$  is MOS transistor gain and it is given by  $\beta = \mu \epsilon / t_{ox} (W/L)$   
 again ' $\mu$ ' is the mobility of the charge carrier  
 ' $\epsilon$ ' is the permittivity of the oxide layer.  
 ' $t_{ox}$ ' is the thickness of the oxide layer.  
 ' $W$ ' is the width of the transistor. ( shown in diagram)  
 ' $L$ ' is the channel length of the transistor.(shown in diagram)

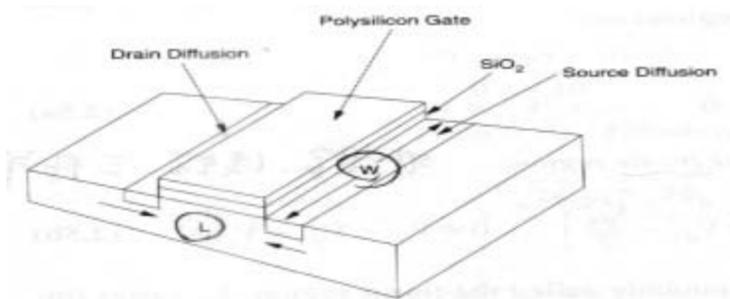


Diagram just to show the length and width of a MOSFET.

The graph of  $I_d$  and  $V_{ds}$  for a given  $V_{gs}$  is given below:

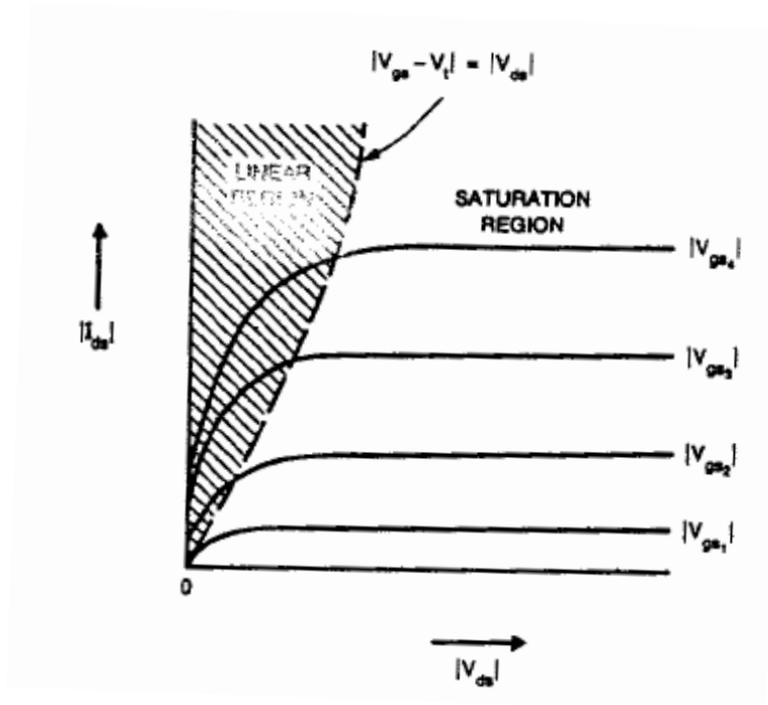


Figure 3: VI Characteristics of MOSFET

## Second Order Effects:

Following are the list of second order effects of MOSFET.

- Threshold voltage – Body effect
- Subthreshold region
- Channel length modulation
- Mobility variation
- Fowler\_Nordheim Tunneling
- Drain Punchthrough
- Impact Ionization – Hot Electrons

### Threshold voltage – Body effect

The change in the threshold voltage of a MOSFET, because of the voltage difference between body and source is called body effect. The expression for the threshold voltage is given by the following expression.

$$V_t = V_{t(0)} + \gamma [(V_{sb} + 2\Phi_F)^{1/2} - (2\Phi_F)^{1/2}]$$

where

$V_t$  is the threshold voltage,

$V_{t(0)}$  is the threshold voltage without body effect

$\gamma$  is the body coefficient factor

$\Phi_F$  is the fermi potential

$V_{sb}$  is the potential difference between source and substrate.

If  $V_{sb}$  is zero, then  $V_t = V_{t(0)}$  that means the value of the threshold voltage will not be changed. Therefore, we short circuit the source and substrate so that,  $V_{sb}$  will be zero.

### Subthreshold region:

For  $V_{gs} < V_t$  also we will get some value of Drain current this is called as Subthreshold current and the region is called as Subthreshold region.

### Channel length modulation:

The channel length of the MOSFET is changed due to the change in the drain to source voltage. This effect is called as the channel length modulation. The effective channel length & the value of the drain current considering channel length modulation into effect is given by,

$$I_{ds} = \frac{\beta}{2} ((V_{gs} - V_t)^2 (1 + \lambda V_{ds}))$$

$$L_{eff} = L - \sqrt{2\epsilon_o \frac{\epsilon_{Si}}{q_i N} (V_{ds} - [V_{gs} - V_t])}$$

Where  $\lambda$  is the channel length modulation factor.

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**Mobility:**

Mobility is defined as the ease with which the charge carriers drift in the substrate material. Mobility decreases with increase in doping concentration and increase in temperature. Mobility is the ratio of average carrier drift velocity and electric field. Mobility is represented by the symbol  $\mu$ .

**Fowler Nordhiem tunneling:**

When the gate oxide is very thin there can be a current between gate and source or drain by electron tunneling through the gate oxide. This current is proportional to the area of the gate of the transistor.

**Drain punchthrough:**

When the drain is a high voltage, the depletion region around the drain may extend to the source, causing the current to flow even if gate voltage is zero. This is known as Punchthrough condition.

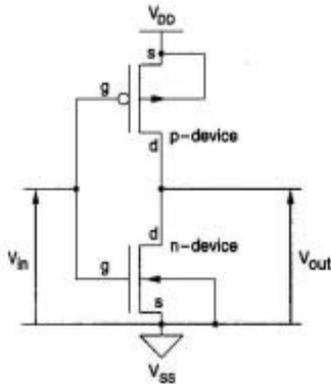
**Impact Ionization-hot electrons:**

When the length of the transistor is reduced, the electric field at the drain increases. The field can become so high that electrons are imparted with enough energy we can term them as hot. These hot electrons impact the drain, dislodging holes that are then swept toward the negatively charged substrate and appear as a substrate current. This effect is known as Impact Ionization.

**MOS Models**

MOS model includes the Ideal Equations, Second-order Effects plus the additional Curve-fitting parameters. Many semiconductor vendors expend a lot of effort to model the devices they manufacture. (Standard : Level 3 SPICE) . Main SPICE DC parameters in level 1,2,3 in 1 $\mu$ m-well CMOS process.

## CMOS INVETER CHARACTERISTICS



**Figure 4: CMOS Inverter**

CMOS inverters (Complementary MOSFET Inverters) are some of the most widely used and adaptable MOSFET inverters used in chip design. They operate with very little power loss and at relatively high speed. Furthermore, the CMOS inverter has good logic buffer characteristics, in that, its noise margins in both low and high states are large.

A CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage VDD at the PMOS source terminal, and a ground connected at the NMOS source terminal, where VIN is connected to the gate terminals and VOUT is connected to the drain terminals.( given in diagram). It is important to notice that the CMOS does not contain any resistors, which makes it more power efficient than a regular resistor-MOSFET inverter. As the voltage at the input of the CMOS device varies between 0 and VDD, the state of the NMOS and PMOS varies accordingly. If we model each transistor as a simple switch activated by VIN, the inverter's operations can be seen very easily:

MOSFET	Condition	on	State	of
	MOSFET		MOSFET	
NMOS	$V_{gs} < V_{tn}$		OFF	
NMOS	$V_{gs} > V_{tn}$		ON	
PMOS	$V_{sg} < V_{tp}$		OFF	
PMOS	$V_{sg} > V_{tp}$		ON	

The table given, explains when the each transistor is turning on and off. When VIN is low, the NMOS is "off", while the PMOS stays "on": instantly charging VOUT to

logic high. When  $V_{in}$  is high, the NMOS is "on" and the PMOS is "off": taking the voltage at  $V_{out}$  to logic low.

### Inverter DC Characteristics:

Before we study the DC characteristics of the inverter we should examine the ideal characteristics of inverter which is shown below. The characteristic shows that when input is zero output will high and vice versa.

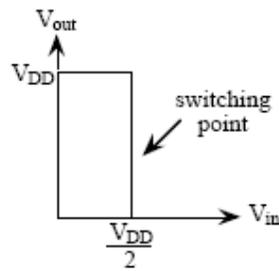


Figure 5: Ideal Characteristics of an Inverter

The actual characteristics is also given here for the reference. Here we have shown the status of both NMOS and PMOS transistor in all the regions of the characteristics.

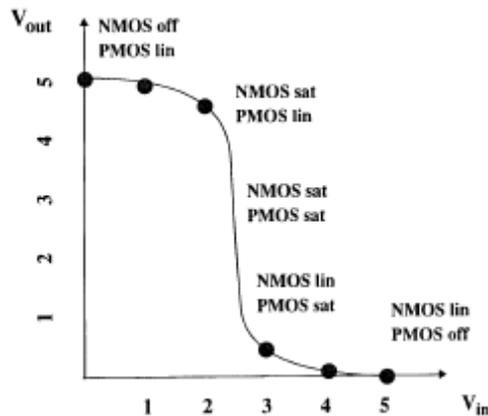


Figure 6: Actual Characteristics of an Inverter

### Graphical Derivation of Inverter DC Characteristics:

The actual characteristics is drawn by plotting the values of output voltage for different values of the input voltage. We can also draw the characteristics, starting with the VI characteristics of PMOS and NMOS characteristics.

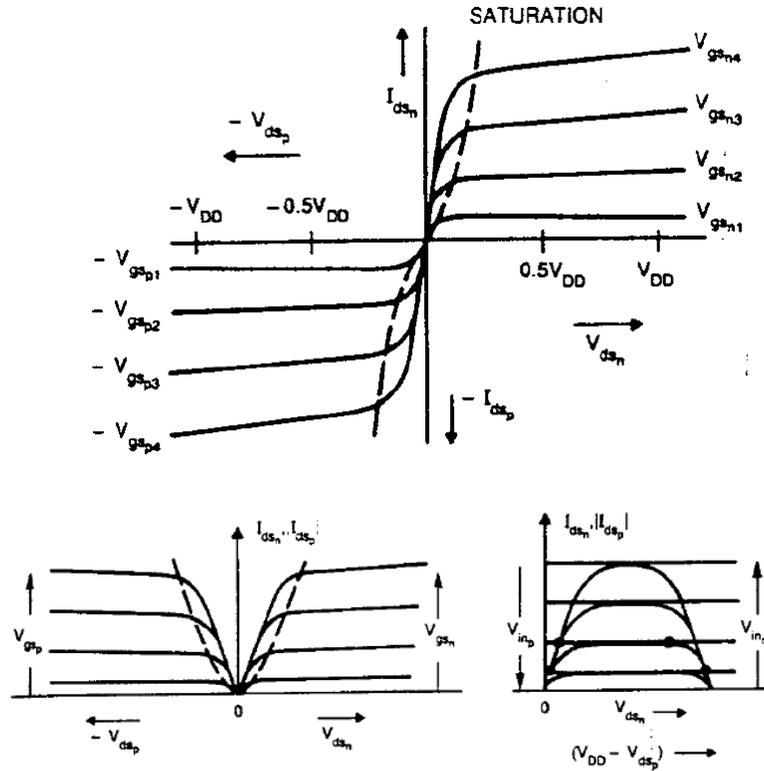


Figure 7a,b,c: Graphical Derivation of DC Characteristics

The characteristics given in figure 7a is the vi characteristics of the NMOS and PMOS characteristics (plot of  $I_d$  vs.  $V_{ds}$ ). The figure 7b shows the values of drain current of PMOS transistor is taken to the positive side the current axis. This is done by taking the absolute value of the current. By superimposing both characteristics it leads to figure 7c. the actual characteristics may be now determined by the points of common Vgs intersection as shown in figure 7d.

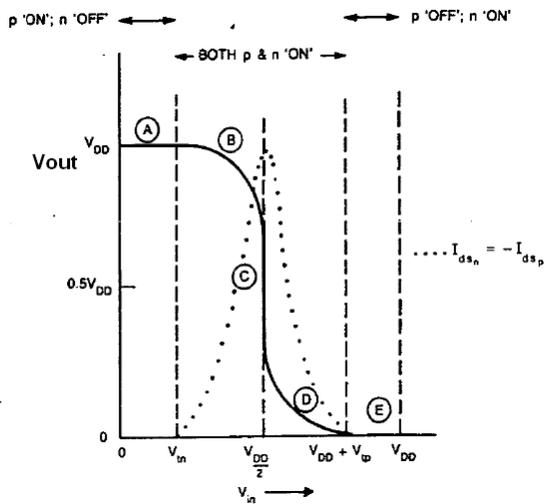


Figure 7d: Cmos Inverter Dc Characteristics

Figure 7d shows five regions namely region A, B, C, D & E. also we have shown a dotted curve which is the current that is drawn by the inverter.

**Region A:**

The output in this region is High because the P device is OFF and n device is ON. In region A, NMOS is cutoff region and PMOS is on, therefore output is logic high. We can analyze the inverter when it is in region B. the analysis is given below:

**Region B:**

The equivalent circuit of the inverter when it is region B is given below.

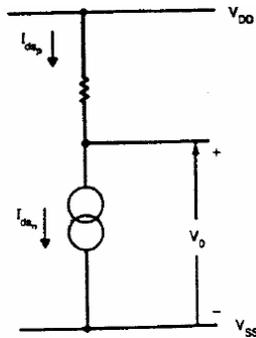


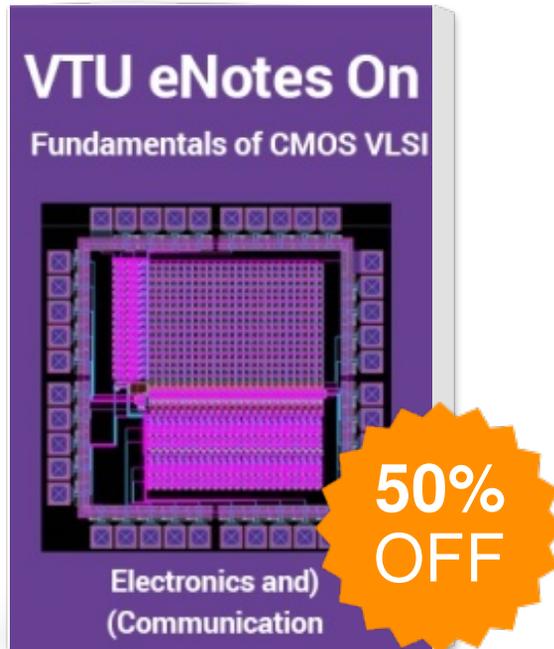
Figure 8: Equivalent circuit in Region B

In this region PMOS will be in linear region and NMOS is in saturation region.

The expression for the NMOS current is 
$$I_{dsn} = \beta_n \frac{[V_{in} - V_{tn}]^2}{2},$$

The expression for the PMOS current is 
$$I_{dsp} = -\beta_p \left[ (V_{in} - V_{DD} - V_{tp})(V_O - V_{DD}) - \frac{1}{2}(V_O - V_{DD})^2 \right]$$

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